


REV A	APPLICATION			REVISIONS		
	PRODUCT LINE	REV	DESCRIPTION	DATE	APPROVED	APPROVED
SH 1	C-2000, P-2000, RT-2000	A	Initial Release per DCA W5962/WPDC118	4/23/07	S. Wild	L. Evans
DWG. NO. 150-049200-05						

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APPROVALS	DATE			TITLE:	
DRAWN Leslie Evans	04/23/07	SERVICE INSTRUCTION, WSI FLEX 2000-04 INSTALLATION OF SOFTWARE MOD 05			
CHECKED Jay Jensen	04/23/07				
PRODUCT MANAGER Scott Hovelsrud	04/23/07				
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ISSUED Leslie Evans	04/23/07	SCALE: NONE		DO NOT SCALE DRAWING	
Typed signatures indicate approval. Handwritten signature approval of this document is on file at Wulfsberg Electronics, Prescott, Arizona.					

SERVICE INSTRUCTION

EQUIPMENT: C-2000, P-2000, RT-2000

DATE: April 23, 2007

INSTRUCTION NUMBER: WSI FLEX 2000-04 Revision A

EFFECTIVITY

All P-2000 assemblies 400-049200-X1-XXX-XXXX-XXXX; all C-2000 assemblies 400-049300-X1-XXX-XXXX-XXXX and all RT-2000 assemblies 400-049400-X1-XXXX-XXXX with software Mod 04 and lower

REASON

To allow installation of Software Mod 05 on P-2000's, C-2000's and RT-2000's.

DESCRIPTION

This service instruction will improve operational characteristics of the unit and improve user reliability of the unit. Some examples include better channel change without lockup, learn mode runs on all configurations, KVL fully operational, OTAR will not cause COMM ERROR, PTT discrete will not cause system to lock up.

COMPLIANCE

On next scheduled maintenance.

WARRANTY INFORMATION

This modification is an enhancement and is covered under warranty.

APPROVAL

This modification does not affect the original approval.

MANPOWER

6.0 hours labor including testing.

REFERENCES

Maintenance Manual, P-2000/C-2000/RT-2000, P/N 150-049004

MATERIAL INFORMATION

The parts required to modify this unit in accordance with this Service Instruction are available from Wulfsberg Electronics at (928) 708-1518.

PARTS REQUIRED

ITEM	QTY	U/M	PART NUMBER	DESCRIPTION	REF
1	1	EA	320-149012-04	SOFTWARE LOAD MODULE, DISPLAY BOARD, PROCESSOR, P-2000	
2	1	EA	320-149015-04	SOFTWARE LOAD MODULE, CPU BOARD, PROCESSOR, P-2000	
3	1	EA	320-149016-04	SOFTWARE LOAD MODULE, CPU BOARD, PLD, P-2000	
4	1	EA	320-149017-02	SOFTWARE LOAD MODULE, DISPLAY BOARD, MAIN PLD, P-2000	
5	1	EA	320-149096-05	SOFTWARE LOAD MODULE, CPU BOARD, FLASH, P-2000	
6	1	RF	150-049004	MAINTENANCE MANUAL, P-2000/C-2000/RT-2000	
7	1	EA	057-03284-0005	LABEL, SOFTWARE CONFIGURATION ID (SW ID)	

MODIFICATION PROCEDURE

- I. If needed, read and archive customer codeplug using CPS software.**
- II. If needed, disassemble unit to gain access to module being updated.**
- III. Load software**

C-2000, P-2000:

Load software modules Item 1 (320-149012-04) and Item 4 (320-149017-02) onto the Display board by following these instructions:

PLD PROGRAMMING

This section describes the programming procedure for the XC95144 Main PLD device installed on the display board of the P-2000/C-2000.

Note: UUT = P-2000 or C-2000 unit being programmed.

REQUIRED HARDWARE

- Power Supply
- TSH-2000 P/N 402-049700
- Xilinx Parallel Cable IV or equivalent
- JTAG Adapter 402-047400
- PC Computer

REQUIRED SOFTWARE

The PC Computer must have the following software installed:

- Xilinx IMPACT V7.1i or equivalent

The following load module file must be available for loading onto the device:

- 320-149017-02.A.JED

This file is located within the load module archive 320-149017-02.A.ZIP. It is recommended the load module file be placed in a temporary working directory, e.g. C:\WORK.

SETUP

The following steps should be followed to prepare the system for programming.

1. Remove the top cover of the UUT.
2. Verify the output of the power supply is 28 VDC +/- 1 VDC.
3. Connect the TSH-2000 to the power supply and to the UUT and leave connected throughout these procedures.
4. Connect the Xilinx Parallel Cable IV between the JTAG Adapter's Xilinx Connector and the PC Parallel Port. Refer to Figure 1 for details of the JTAG Adapter.
5. Connect the JTAG Adapter's 20-pin Programming Cable to the 20-pin connector on the display board.
6. Turn the TSH-2000 Power ON and if needed, the UUT ON.

PROGRAMMING

To program the PLD, proceed as follows.

1. Run the Xilinx IMPACT Program software.
2. Select **File -> Initialize Chain** from the main menu.
3. Double click on the XC95144 chip icon and select the file **320-149017-02.A.JED** as determined above.
4. Single click on the XC95144 chip icon.
5. Select **Operations -> Program**, from the main menu. Ensure the "Erase Before Programming" and "Verify" options are checked in the ensuing **Options** dialog, then select **OK**.
6. Wait for the message "All operations were completed successfully" to appear on the display. Any other result constitutes a failure.
7. Select **OK**.

If a failure occurs, exit the JTAG program, verify all connections are correct, cycle power on the display board, and retry the load per the instructions above.

VERIFICATION

To verify the device was successfully programmed, do the following:

1. Single click on the chip icon.
2. Select **Operations -> Get Device Checksum** from the main menu.
3. Verify the Checksum value displayed during test is 20CA.
4. Select **OK** on the JTAG display.

FINISH

1. Exit the IMPACT program.
2. Power the UUT OFF using the TSH-2000 power switch.
3. Disconnect the Xilinx Parallel Cable's leads from the display board.
4. Restart computer to access parallel port.

DISPLAY MICROPROCESSOR PROGRAMMING

This section describes the programming procedure for the microprocessor device installed on the display board of the P-2000/C-2000.

REQUIRED SOFTWARE

The PC Computer must have the following software installed:

- Intel JFLASHMM utility WED 320-449112-5107 SOFTWARE, COMMERCIAL, INTEL, JFLASH, V5.01.007

The following load module file must be available for loading onto the device:

- 320-149012-04.A.BIN

This file is located within the load module archive 320-149012-04.A.ZIP. It is recommended the load module file be placed in a temporary working directory, e.g. C:\WORK.

SETUP

The following steps should be followed to prepare the system for programming.

1. Connect the DSUB 25 pin Cable between the JTAG Adapter Parallel Port Connector and the PC Parallel Port. Refer to Figure 1 for details of the JTAG Adapter.
2. Connect the JTAG Adapter's 20-pin ribbon cable to the 20-pin connector on the display board.
3. Power the UUT ON using the TSH-2000 power switch.

PROGRAMMING

To program the microprocessor, proceed as follows:

1. Open a command prompt (DOS box) on the PC computer.
2. Change the current directory to the location where the JFLASHMM utility was stored, using the following command:
CD C:\Program Files\Intel Corporation\JFlash_MM.
3. Execute the JFLASHMM utility using a command similar to the following, but using the actual load module file name:

```
JFLASHMM DBCX52 C:\WORK\320-149012-04.A.BIN P 0 PAR
```

Note: If this command fails, repeat the above command 2-3 times. If the problem persists, verify all connections are correct, cycle power on the system, and retry the load per the instructions above.

4. The screen will indicate the progress of the programming operation. Wait until it shows the load was completed successfully.

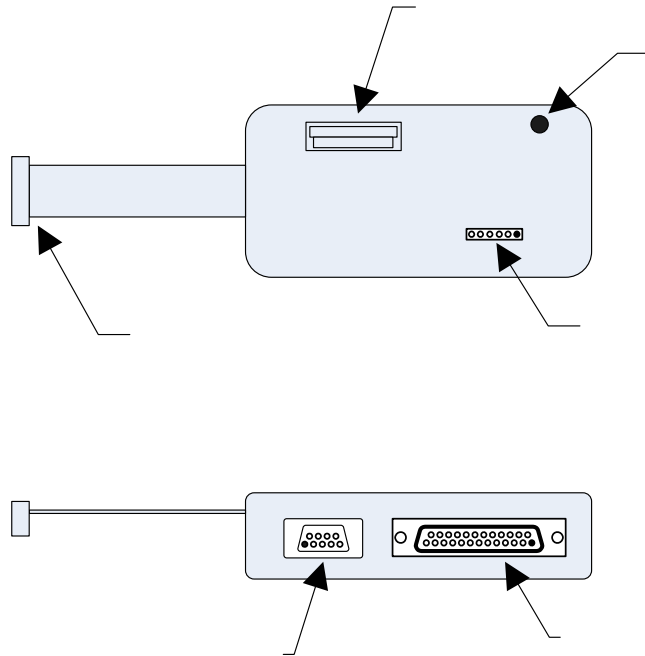
If a failure occurs, verify all connections are correct, cycle power on the display board, and retry the load per the instructions above.

VERIFICATION

The JFLASHMM utility automatically verifies the loaded image. Verify the utility reports no errors and a successful verification.

FINISH

1. Exit the command prompt (DOS box).
2. Power the UUT OFF using the TSH-2000 power switch.
3. Disconnect the JTAG Adapter's 20-pin Programming Cable from the display board.



20-Pin Programming Cable	The small 20-pin ribbon cable is connected to the 20-pin header on the processor board
Xilinx (CPLD/FPGA) Connector	The Xilinx Cable is connected from the Xilinx Pod to this header
Parallel Port Connector	The Parallel port cable is connected from the PC to this connector
Serial Port Connector	The Serial Port connector is not used in this application.
Interface Board Connector	The Interface Board Connector is not used in this application
Power on LED	The Power on LED indicated that the unit is powered and ready to operate.

Figure 1 JTAG Adapter Board 402-047400-02

P-2000, C-2000, RT-2000:

Load software modules Item 2 (320-149015-04) and Item 3 (320-149016-04) and Item 5 (320-149096-05) on the CPU board by following these instructions:

XC95288 CPLD PROGRAMMING

PURPOSE

This section describes the programming procedure for the XC95288 CPLD installed on the CPU board of the P-2000/RT-2000/C-2000.

PROCEDURE

Note: UUT = P-2000 or RT-2000 or C-2000 unit being programmed.

REQUIRED HARDWARE TEST EQUIPMENT

- +28 VDC 1 Amp Power Supply
- TSH-2000 P/N 402-049700
- P-2000 RS232 Test Cable P/N 124-049232
- Xilinx Parallel Cable IV or equivalent
- PC Computer

REQUIRED SOFTWARE

The PC Computer must be loaded with the following software:

- Xilinx IMPACT V7.1i or equivalent

The following load module file must be available for loading onto the Cpu Board:

- 320-149016-04.A.JED

This file is located within the load module archive 320-149016-04.A.ZIP. It is recommended the load module and the 320-149016.A.cdf file be placed in a temporary working directory, e.g. C:\WORK.

SETUP

The following steps should be followed to prepare the system for programming.

1. Connect the Xilinx Parallel Cable's leads to the corresponding pins on the 20 pin connector A3J9 on the cpu board (See Table 1).

Xilinx Parallel Cable Pin	Cpu Board Pin A3J9
TMS	15
TDI	16
TDO	17
TCK	18
GND	19
+5VDC	20

2. Carefully connect a jumper between pins 2 and 3 of Q905. Leave this jumper in place for the remainder of these tests.
3. Power the UUT ON using the TSH-2000 power switch.

PROGRAMMING

To program the PLD, proceed as follows.

1. Run the Xilinx IMPACT V7.1i software.
2. Select **File -> Initialize Chain** from the main menu.
3. Double click on the XC95288 chip icon and select the file **320-149016-04.A.JED** as determined above.
4. Single click on the XC95288 chip icon.
5. Select **Operations -> Program**, from the main menu. Ensure the "Erase Before Programming" and "Verify" options are checked in the ensuing **Options** dialog, then select **OK**.
6. Wait for the message "All operations were completed successfully" to appear on the display. Any other result constitutes a failure.
7. Select **OK**.

If a failure occurs, exit the IMPACT program, verify all connections are correct, cycle power on the display board, and retry the load per the instructions above.

VERIFICATION

To verify the device was successfully programmed, do the following:

1. Single click on the chip icon.
2. Select **Operations** -> **Get Device Checksum** from the main menu.
3. Verify the Checksum value displayed during test is 0EBC.
4. Select **OK** on the IMPACT display.

POWER DOWN

1. Close the program.
2. Power the UUT OFF using the TSH-2000 power switch.
3. Remove connections to A3J9 on cpu board.

XA-G49 PROGRAMMING

PURPOSE

This section describes the programming procedure for the XA-G49 Processor installed on the CPU board of the P-2000/RT-2000/C-2000.

REQUIRED SOFTWARE

The PC Computer must be loaded with the following software:

- Phillips In System Programmer V2.24 or equivalent
- Terminal Emulator - Microsoft HyperTerminal or equivalent

The following load module file must be available for loading onto the Cpu Board:

- 320-149015-04.A.HEX

This file is located within the load module archive 320-149015-04.A.ZIP. It is recommended the load module file be renamed cpuint.hex and be placed in a temporary working directory, e.g. C:\WORK.

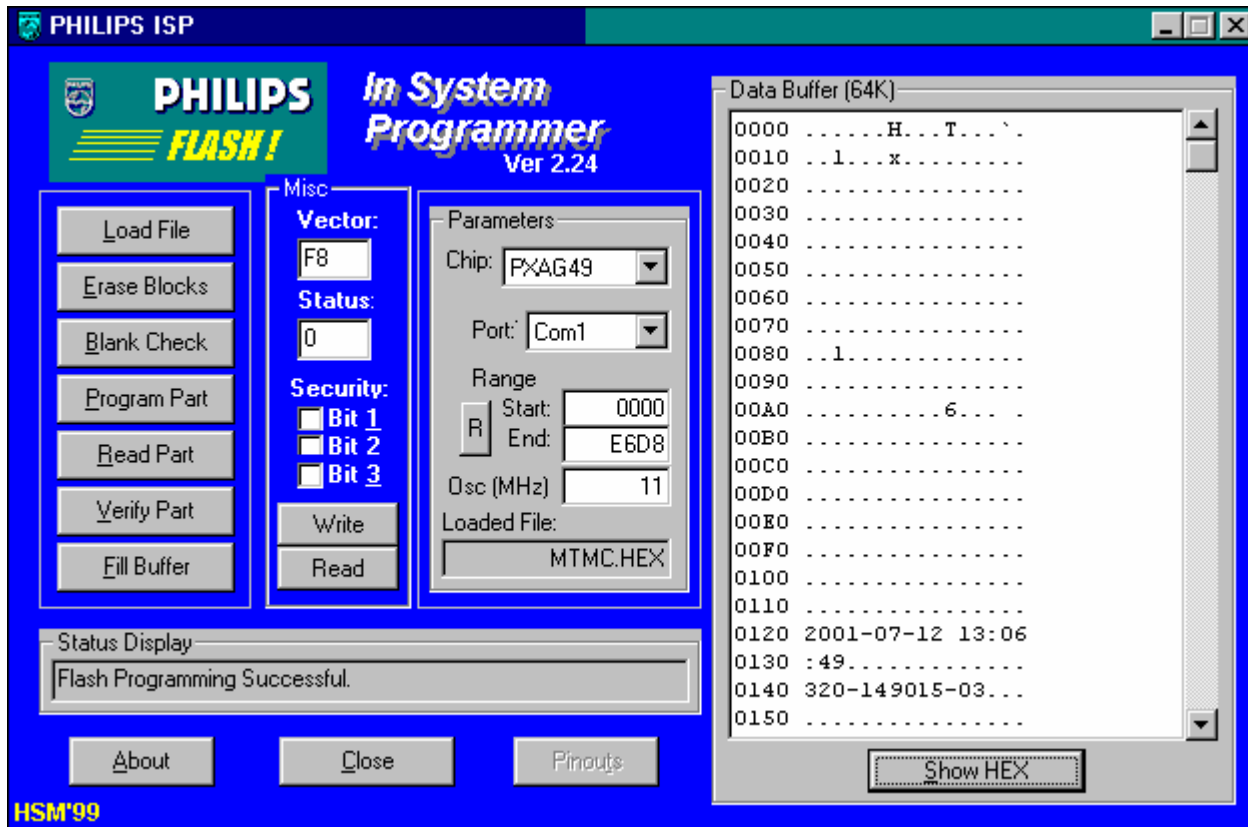
TEST SETUP

1. Insure the TSH-2000 power switch for the UUT power is OFF.
2. Connect the RS232 Test Cable between the PC COM 1 and the UUT connector J102.
3. Turn RS232 Test Cable switches S1 OFF, S2 and S3 ON.

PROGRAMMING

See Figure 2 for a typical display (for reference only) for the Phillips 'In System Programmer' V2.24 software.

Figure 2: Phillips 'In System Programmer' V2.24 Software Display



NOTE: There MUST be a valid program in the XC95288 before the XAG49 can be programmed.

The 'In System Programmer' display is divided into several different areas. We will be using **Parameters**, **Misc**, **Data Buffer**, the buttons on the left of the display, and the **Status Display** near the bottom.

1. Power the UUT ON using the TSH-2000 power switch.
2. Run the Phillips 'In System Programmer' V2.24 software by double clicking on the WINISP icon. Select or enter the following under **Parameters**:
 - Chip - PXAG49
 - Port - Com1
 - Osc (MHz) - 24
3. Select **Read** under the **Misc** area.
 - You must get a 'Boot Vector Read OK' in the **Status Display** before continuing. If this test fails, check all hardware connections and cables.
4. Under the **Misc** area:
 - If the Status box is zero '0', skip to step 5.
 - If the Status box is NOT zero '0', enter zero '0'.
 - Select **Write**.
 - When the 'Status Byte Change Confirmation' message is displayed, select **Yes**.
 - When complete the **Status Display** will show 'Boot Vector Programmed OK'.
5. Select **Load File**
 - Select file **cpuint.hex**.
 - If file load is successful, the **Status Display** will show 'File Loaded OK' and the **Parameters** area will show 'Loaded File': **cpuint.hex**.

6. Select **Erase Blocks**

At the 'Block Erase Selection' display, select **Full Chip Erase**.

At the 'Full Erase Confirmation' screen, select **Yes**.

A Status Display of 'Chip Fully Erased' will be displayed if successful.

NOTE: This will take about 15 seconds. Do NOT select anything else during this time.

7. Select **Program Part**

Status of 'Programming Flash' will be displayed in the **Status Display** area during the actual programming.

A status of 'Flash Programming Successful' will be displayed if successful.

ANY other status constitutes a FAILURE.

NOTE: This will take about 5 minutes to complete. Do NOT select anything else during this time.

SOFTWARE VERSION CHECK

At the bottom of the **Data Buffer** area of the display, select the button until it reads 'Show HEX'. The button toggles between 'Show ASCII' and 'Show HEX'. Verify that the line at about address 0120 displays the revision date of 2005-09-20 and the line at about address 0140 displays part number 320-049015-04.

POWER DOWN

1. Close the program.
2. Power the UUT OFF using the TSH-2000 power switch.

FLASH PROGRAMMING

PURPOSE

This section describes the programming procedure for the Flash installed on the CPU board of the P-2000/RT-2000/C-2000.

REQUIRED SOFTWARE

The PC Computer must be loaded with the following software:

- Tera Term program or equivalent

The following load module file must be available for loading onto the Cpu Board:

- 320-149096-05.A.HEX

This file is located within the load module archive 320-149096-05.A.ZIP. It is recommended the load module file be renamed `cpuext.hex` and be placed in a temporary working directory, e.g. C:\WORK.

TEST SETUP

1. Insure UUT power is OFF.
2. Insure the RS232 Test Cable is connected between the PC COM 1 and the UUT connector J102.
3. Turn ALL RS232 Test Cable switches OFF.

PROGRAMMING

1. Run the Tera Term program. Be sure baud rate is set to 38400.
2. Power the UUT ON using the TSH-2000 power switch.
3. As soon as the message "Press BACKSPACE now to access Int Flash Menu" appears, press the BACKSPACE key on the keyboard.
Note: It may take several attempts to get the timing right. If 'garbage' characters appear, re-cycle power and try again.
4. If successful, you will get the '29F200 Flash Loader Program' display. Press ENTER and wait for 'Waiting For Data From PC...' prompt.
5. Select **File** -> **Send File** from the main menu and **Open** the file 'cpuext.hex'.
6. Wait for the 'Download Complete' message to appear in about 3 minutes.
7. The Cpu Board will reset and return to the command prompt (P2K> or C2K> or RT2K>) and begin running.

SOFTWARE VERSION CHECK

1. Using the terminal emulator connected to the UUT, type in **ver** and press **RETURN** to display the currently loaded software and verify that the data on the display has the correct Part Number (320-149096-05) and date (2007-04-20).
2. Using the terminal emulator connected to the UUT, type in **ef user** and press **RETURN**.

POWER DOWN

1. Close the program.
2. Insure UUT power is OFF.
3. Disconnect all test equipment from UUT.
4. Re-assemble UUT.

IV. Configure/Test:

Using Item 6 - Maintenance Manual, P-2000/C-2000/RT-2000, run the following sections on the UUT:

Section 3 Maintenance

Section 3.6.B UUT Setup

Section 3.6.C Transmitter Alignment

Section 3.6.D Preliminary Audio Setup

Section 3.7 Final Acceptance Test

NOTE: Use of these updated boards require the LRU to have SWID -05 label 057-03284-0005 (item 7).

V. If needed, restore customer codeplug using CPS software.

VI. Single Tanapa Unit:

This Service Instruction authorizes the creation of the following single tanapa P-2000 / RT-2000:

400-049200-AB-CDE-WWWW-0000 Final Assembly, P-2000

400-049400-AB-CDE-WWWW-0000 Final Assembly, RT-2000

where AB-CDE-WWWW is defined in Table 1.

Table 1: Definition of P-2000 / RT-2000 Part Number (Ref 149-149001)

400-049200-AB-CDE-XXXX P-2000
400-049400-AB-CDE-XXXX RT-2000

- A: Major Hardware Variation**
1 = Initial Release
- B: Major Software Variation**
1 = Initial Release
- C: Reserved for future use (Always marked "0")**
- D: Faceplate Option**
1 = Black Face Plate
2 = Grey Face Plate
- E: Display Option**
1 = Standard Display
2 = NVG Compatible Display

WWWW: FM1 Options

W W W W

			-----Encryption
			-----Trunking
			0 = None
			1 = Multikey, DES/DES-XL/DES-OFB, OTAR
			2 = DVP-XL, OTAR
			3 = DVI-XL, OTAR
			4 = Multikey, AES, OTAR
			5 = Multikey, AES/DES/DES-XL/DES-OFB, OTAR
			6 = Multikey, DES/DES-XL/DES-OFB
			-----Frequency Band
			0 = None
			1 = 137 - 174 MHz
			2 = 403 - 470 MHz
			3 = 450 - 520 MHz
			4 = 806 - 870 MHz
			5 = 380 - 470 MHz
			6 = 764 - 870 MHz
			-----ITM
			0 = 255 Channels (XTS-3000)
			1 = 240 Channels (XTS-5000), Front Panel Programmable (FPP)
			2 = 512 Channels (XTS-5000)

XXXX: FM2 Options

X X X X

			-----Encryption
			-----Trunking
			0 = None
			1 = Multikey, DES/DES-XL/DES-OFB, OTAR
			2 = DVP-XL, OTAR
			3 = DVI-XL, OTAR
			4 = Multikey, AES, OTAR
			5 = Multikey, AES/DES/DES-XL/DES-OFB, OTAR
			6 = Multikey, DES/DES-XL/DES-OFB
			-----Frequency Band
			0 = None
			1 = 137 - 174 MHz
			2 = 403 - 470 MHz
			3 = 450 - 520 MHz
			4 = 806 - 870 MHz
			5 = 380 - 470 MHz
			6 = 764 - 870 MHz
			-----ITM
			0 = 255 Channels (XTS-3000)
			1 = 240 Channels (XTS-5000), Front Panel Programmable (FPP)
			2 = 512 Channels (XTS-5000)